# Priyank Faldu

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## Career at a Glance

In my career spanning PhD and ~4 years of industry experience, I have predominantly worked on projects related to performance modeling of CPU/GPU architectures and cache subsystems. The projects also covered various aspects of systems research that included software-hardware co-design [HPCA'20, Patent #10,417,134], design of novel microarchitecture mechanisms [PACT'17], simulation driven bottleneck/efficiency analysis of microarchitecture components [WDDD'16], characterization and software optimization of emerging applications for an existing hardware architecture [IISWC'19], and accelerating applications using GPU via OpenCL/CUDA and other parallel programming paradigms [Patent #9,727,382]. Several of these projects led to successful publications in top-tier architecture conferences, patents, a grant and an award.

## Research Interests

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|---|---|
| Broad | Computer systems and the interaction between software and hardware |
| Current Focus | Computer architecture, Performance modeling, Software-hardware co-design |

## Education

Oct. 2014 – Jun. 2020, Edinburgh, UK
**Doctor of Philosophy**, Informatics, The University of Edinburgh
Thesis: "*Addressing Variability in Reuse Prediction for Last-Level Caches*"
Advisor: Prof. Boris Grot

Jul. 2008 – Jun. 2010, Kanpur, India
**Master of Technology**, Computer Science and Engineering, IIT Kanpur
Thesis: "*CUDA-LF: A Lock-Free Data Structure Library for GPGPU*"
Advisor: Prof. Mainak Chaudhuri
CGPA: 10/10

Jul. 2004 – May 2008, Ahmedabad, India
**Bachelor of Technology**, Computer Engineering, Nirma University
CGPA: 8.39/10

## Work Experience

May 2016 – Sep. 2016, Austin, USA
**Oracle Labs**, Research Intern
Part of the Performance Modeling, Simulation, and Optimization team. I worked on designing high-performance mechanisms and polices for managing the last-level caches to accelerate graph-analytic applications, which materialized into a successful patent.

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|---|---|
| Language | C++ |
| Scope | Performance modeling, Microarchitecture exploration |

Jul. 2013 – Aug. 2014, Bangalore, India
**Samsung R&D Institute India**, Lead Engineer
Part of the Android Graphics team responsible for exploring the opportunities for accelerating multimedia applications on the company's flagship Galaxy smartphone devices using OpenCL. We ported two multimedia applications – HDR and Bokeh – on GPUs, reducing the application runtime over their highly optimized CPU implementations and accelerated PNG encoder & decoder implementation on CPU by devising a software multi-threading strategy.

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|---|---|
| Language | C, C++, OpenCL, Pthread |
| Scope | Application characterization, Performance acceleration (GPU & CPU) |

## Work Experience (Cont.)

May 2011 – Jul. 2013 **Intel Technology India Pvt. Ltd.**, Graphics Hardware Engineer
Bangalore, India Part of the path-finding team responsible for proposing new features and analyzing feasibility of the proposed features for GPGPU pipeline of future generation integrated-GPU architectures. I worked on the development of various simulation tools to facilitate the OpenCL workload characterization studies.
Language C++
Scope Simulator development, Performance modeling

Jul. 2010 – Mar. 2011 **Google India Pvt. Ltd.**, Software Engineer
Bangalore, India Part of the Google Map Maker product team. I worked on the development of various UI features and a module to analyze user-engagement.
Language C++, JavaScript, MapReduce
Scope Web development

## Patents

US20180129613A1 "*Cache Memory Architecture and Policies for Accelerating Graph Algorithms*"
May 2018 **P. Faldu**, J. Diamond, and A. Patel
Assignee Oracle International Corporation
Language C++ (Sniper simulator)
Scope Performance modeling, Microarchitecture exploration, Software-hardware co-design

US20160004570A1 "*Parallelization Method and Electronic Device Based on Profiling Information*"
Jan. 2016 J. Koh, A. Oberoi, G. P. Sharma, R. Velappan, and **P. Faldu**
Assignee Samsung Electronics Co., Ltd.
Language C, C++, OpenCL
Scope Application characterization, Performance acceleration (GPU)

## Peer-Reviewed Publications

HPCA 2020 "*Domain-Specialized Cache Management for Graph Analytics*" **P. Faldu**, J. Diamond, and B. Grot
In Proceedings of the 26th International Symposium on High-Performance Computer Architecture.
Language C++ (Sniper simulator)
Scope Performance modeling, Microarchitecture exploration, Software-hardware co-design

IISWC 2019 "*A Closer Look at Lightweight Graph Reordering*" **P. Faldu**, J. Diamond, and B. Grot
In Proceedings of the International Symposium on Workload Characterization.
Language C++, OpenMP
Scope Application characterization, Performance acceleration (CPU)

PACT 2019 "*POSTER: Domain-Specialized Cache Management for Graph Analytics*" **P. Faldu**, J. Diamond, and B. Grot
In Proceedings of the 28th International Conference on Parallel Architectures and Compilation Techniques.
Language C++ (Sniper simulator)
Scope Performance modeling, Microarchitecture exploration, Software-hardware co-design
**Awarded first place in the ACM Student Research Competition (SRC).**

## Peer-Reviewed Publications (Cont.)

PACT 2017 "*Leeway: Addressing Variability in Dead-Block Prediction for Last-Level Caches*" **P. Faldu**, and B. Grot
In Proceedings of the 26th International Conference on Parallel Architectures and Compilation Techniques.
Language C++ (CMP$im & Flexus simulators))
Scope Performance modeling, Microarchitecture exploration

CRC 2017 "*Reuse-Aware Management for Last-Level Caches*" **P. Faldu**, and B. Grot
In 2nd International Cache Replacement Championship Workshop at ISCA.
Language C++ (ChampSim simulator)
Scope Performance modeling, Microarchitecture exploration

WDDD 2016 "*LLC Dead Block Prediction Considered Not Useful*" **P. Faldu**, and B. Grot
In 13th International Workshop on Duplicating, Deconstructing and Debunking at ISCA.
Language C++ (CMP$im simulator)
Scope Performance modeling, Bottleneck/efficiency analysis

## Academic Achievements

2019 Awarded first place in the *ACM Student Research Competition (SRC)* at PACT conference for our work on a hardware/software co-design to accelerate graph analytics.

2008–09 Received *Academic Excellence Award* at IIT Kanpur.

2008–10 Topper of the M. Tech. batch at IIT Kanpur.

2008 All India Rank 263 (of 18224 candidates) in *Graduate Aptitude Test in Engineering (GATE)* for the Computer Science discipline.

## Grants

2017 "*Efficient Scale-Up Graph Processing on Future Memory Systems*"
**Oracle ERO Award**: $76,000
Co-authored the grant proposal with Prof. Boris Grot (sole PI).

## Professional Services

2019 **Journal Reviewer**: IEEE Computer Architecture Letters (CAL)

2018 **Organizing Committee Member**: Web co-chair of the International Symposium on Computer Architecture (ISCA)

## Mentoring Experience

**Honours Project**, The University of Edinburgh
Sep. 2017 – Apr. 2018 Elitsa Bankova, The University of Edinburgh, UK
Sep. 2016 – Mar. 2017 Keith Donaldson, The University of Edinburgh, UK

**Research Internship**, The University of Edinburgh
Jul. 2018 – Aug. 2018 Kuntai Du, Peking University, China
Jun. 2018 – Nov. 2018 Adam McCabe, The University of Edinburgh, UK
Jul. 2017 – Jan. 2018 Pramod Chunduri, IIT Kanpur, India

**Industry Internship**, Samsung R&D Institute India
May 2014 – Jul. 2014 Rajat Sinha, IIT Guwahati, India

**Industry Internship**, Intel Technology India Pvt. Ltd.
Jun. 2012 – Apr. 2013 Shruti Pavagadhi, Nirma University, India
May 2011 – May 2012 Akhila Surishetti, NIT Warangal, India